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LERNER AND GREENBERG, P.A.			EXAMINER	
Post Office Box 2480 Hollywood, FL 33022-2480			PAREKH	, NITIN
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			2811 DATE MAILED: 06/26/2003	Ϊζο

Please find below and/or attached an Office communication concerning this application or proceeding.

r.	Applicati n N .	Applicant(s)				
· _	09/833,260	HACKE, HANS-JURGEN				
Offic Action Summary	Examiner	Art Unit				
	Nitin Parekh	2811				
Th MAILING DATE of this communication appears on the cover sh et with the correspondenc address Peri d for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status						
1) Responsive to communication(s) filed on 21	April 2003 .					
2a)⊠ This action is FINAL . 2b)□ T	his action is non-final.					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. Disposition of Claims						
4) Claim(s) <u>52-71 and 78-107</u> is/are pending in	the application.					
4a) Of the above claim(s) 78-104 is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6) Claim(s) <u>52-71 and 105-107</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and	or election requirement.					
Application Papers						
9)☐ The specification is objected to by the Examiner.						
10)⊠ The drawing(s) filed on <u>10 April 2001</u> is/are: a)⊠ accepted or b)⊡ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner.						
If approved, corrected drawings are required in reply to this Office action.						
12)☐ The oath or declaration is objected to by the Examiner.						
Pri rity under 35 U.S.C. §§ 119 and 120						
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a)⊠ All b)□ Some * c)□ None of:						
 Certified copies of the priority document 	nts have been received.					
2. Certified copies of the priority documen	nts have been received in Applicati	ion No				
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
	•					
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).						
 a) ☐ The translation of the foreign language provisional application has been received. 15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121. 						
Attachment(s)	_					
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)						
S. Patent and Trademark Office						

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DETAILED ACTION

Claim R j ctions - 35 USC § 112

- 1. The following is a quotation of the second paragraph of 35 U.S.C. 112:
 - The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 2. Claims 59 and 61 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
- A. Claim 59, lines 2-5 cite: "... wherein said <u>surface</u> of the said substrate has <u>a</u> <u>largest bulging area</u> and said contact element has a <u>length</u> that is at least 5% greater than said largest <u>bulging area</u> of said surface of said substrate."

It is not clear how a value/number of the bulging of the <u>surface area</u> (square mm, square inch, etc.) is numerically compared with the linear dimension (mm, inch, etc.) of the contact element since the units of the area and length are not the same.

B. Claim 61, lines 3- 6 cites: ".....said contact element having a length being at least 5% greater than the largest length difference with regard to said centrally located neutral point of the substrate in event of maximum thermal cycling".

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It is not clear from the description in the specification what conditions and parameters are referred to define "maximum thermal cycling" so that a dimensional comparison can be made with respect to the length dimension.

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 52-71 and 105-107 are rejected under under 35 U.S.C. 103(a) as being unpatentable over Khandros et al. (US Pat. 5917707).

Regarding claim 52, Khandros et al. disclose an electronic component/device/circuit having a contact structure, the device comprising:

- a substrate/silicon wafer package/active chip device (102 in Fig. 2; Col. 4, line
 18) having a surface (104 in Fig. 2)
- and the circuit including a plurality of contact areas/pads (103 in Fig. 2; Col. 4, lines 13-40), the contact areas having microscopically small dimensions ranging from 2-50 mils (Col. 4, line 40), and

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- the contact area including microscopically small flexible contact element (122 in Fig. 2) having microscopically small dimension/length ranging from 10-500 mils (Col. 4, line 58), and
- the contact element having a base (126 in Fig. 2) and a part integrally provided/formed with the base (Col. 4, line 65), the part extending from the contact area in three dimensions (123/124/127 in Fig. 2) in a direction deviating from a direction parallel to the electronic circuit/device surface on the substrate and being angularly disposed in a multiple bends/angles (Col. 6, line 45-58) relative to the substrate in an unstressed condition

(Fig. 1 and 2; Col. 4, line 13- Col. 7, line 17).

Khandros et al. fail to specify the device/electronic circuit having interconnects being formed on the surface of the substrate.

Khandros et al. further teach an embodiment in Fig. 6 where the device has a plurality of contact areas and interconnects/through-hole connections (158 in Fig. 6) having ends (see top/bottom portions of 158 in Fig. 6) where each contact area is configured for respective interconnect (Col. 8, lines 5-35).

it would have been obvious to a person of ordinary skill in the art at the time invention was made to the device/electronic circuit having interconnects being formed on the surface of the substrate so that the desired electrical routing/interconnection for each contact element can be achieved in Khandros et al's device.

Regarding claim 53, Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, and further teach the contact area/element of the device being configured opposite the connection area of an intermediate carrier/printed circuit board (PCB) (411 in Fig. 25) having a flat conductors/pads (413 in Fig. 25; Col. 16, line 60- Col. 17, line 14).

Regarding claim 54, Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, including the substrate being a semiconductor chip having an electronic circuit on/near the surface of the substrate (103 in Fig. 2; Col. 4, lines 13-40).

Regarding claim 55, Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, including the plurality of interconnects having ends and each of the contact areas/elements being configured on the respective ends of each of the interconnects (Fig. 6; Col. 8, lines 5-35).

Regarding claim 56, Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, including the contact elements being elastically deformable/flexible (Col. 6, line 39).

Regarding claims 57 and 58, Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, including the contact element (122 in Fig. 2) being formed/preformed/prebent at various different angles/bends and shapes deviating from a direction orthogonal to the substrate surface (Col. 6, lines 35-60).

Regarding claim 59, Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, except the contact element having a length being at least 5% greater than the largest budging dimension of the substrate.

The determination of parameters such as dimensions (length, width, etc.) of the contact element/lead, contact area/pad (shape, cross-section, etc.) interconnect wiring//trace, number of contact elements/leads, pitch/spacing, etc. and their effect/interaction due to thermal processing, thermal cycling, differences in thermal expansion of various material, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired contact resistance, surface connection area, and connection flexibility.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the contact element having a length being at least 5% greater than the largest the largest bulging dimension of the substrate so that the desired contact resistance, interconnect reliability and the bonding strength can be achieved in Khandros et al's device.

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Regarding claim 60, Khandros et al. teach substantially the entire claimed structure as applied to claims 52 and 53 above, including the contact element having a length being 5% greater than the largest distance between the contact areas of the device and the intermediate carrier/PCB (see 418 between 416 and 411 in Fig. 25).

Regarding claim 61, Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, except the contact element having a length being at least 5% greater than the largest length difference with regard to a centrally located neutral point (CNP) of the substrate in an event of maximum thermal cycling.

The determination of parameters such as dimensions (length, width, etc.) of the contact element/lead, contact area/pad (shape, cross-section, etc.) interconnect wiring//trace, number of contact elements/leads, pitch/spacing, etc. and their effect/interaction due to thermal processing, thermal cycling, differences in thermal expansion of various material, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired contact area, connection flexibility and interconnect density.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the contact element having a length being at least 5% greater than the largest length difference with regard to a centrally located neutral point (CNP) of the substrate in event of maximum thermal cycling so that the desired contact

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resistance, surface connection area, and connection flexibility can be achieved in Khandros et al's device.

Regarding claim 62, Khandros et al. teach substantially the entire claimed structure as applied to claims 52, 53 and 61 above, including the device being in combination with the intermediate carrier/printed circuit board (PCB-411 in Fig. 25) having the flat conductors/pads (413 in Fig. 25; Col. 16, line 60- Col. 17, line 14).

Regarding claim 63, Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, and further teach using the same metal/alloy as gold for the contact element and the pad/contact area to achieve low resistance for the contact structure (Col. 16, line 10).

Regarding claim 64, Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, and further teach using the contact structure having gold (Col. 16, line 10) as the contact element and a conventional aluminum metal/alloy pad/contact area (Col. 16, lines 10-15).

Regarding claim 65, Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, and further teach using the contact structure having copper

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(Col. 6, line 66) as the contact element and a conventional aluminum metal/alloy pad/contact area (Col. 16, lines 10-15).

Regarding claim 66, Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, and further teach the contact structure being such that the contact element can be designed/reconfigured as a contact pin (106 in Fig. 1) having an end with a contact head (112 in Fig. 1; Col. 6, line 26; Col. 8, line 51).

Regarding claim 67, Khandros et al. teach substantially the entire claimed structure as applied to claims 52, 53 and 66 above, except the contact pin having a diameter being not greater than half of the shortest linear dimension of the contact area.

However, as explained above, the determination of parameters such as dimensions of the contact element/lead including a diameter/length, contact area/pad, interconnect wiring//trace, number of contact elements/leads, pitch/spacing, etc. and their effect/interaction due to thermal processing, thermal cycling, differences in thermal expansion of various material, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired contact resistance, surface connection area, connection flexibility and reduced bonding defects.

it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the contact pin having a diameter being not greater than

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half of the shortest linear dimension of the contact area so that electrical shorting and bonding defects can be prevented in Khandros et al's device.

Regarding claim 68, Khandros et al. teach substantially the entire claimed structure as applied to claims 52, 53, 62 and 66 above, and further teach the pin being remote from the contact area (112/101 in Fig. 1).

Regarding claim 69, Khandros et al. teach substantially the entire claimed structure as applied to claims 52, 66 and 68 above, and further teach using the contact pin including a head being formed with a gold or lead/tin solder coating (Col. 4, lines 46-51).

Regarding claim 70, Khandros et al. teach substantially the entire claimed structure as applied to claims 52, 66 and 68 above, and further teach using the contact pin including a head being formed with a gold or lead/tin solder coating (Col. 4, lines 46-51).

Regarding claim 71, Khandros et al. teach substantially the entire claimed structure as applied to claims 52, 66, 68 and 70 above, including the contact pin being remote from the contact area (112/101 in Fig. 1).

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Regarding claim 105, Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, and further teach:

- the contact structure being such that the contact element can be designed/reconfigured as a contact pin or pin-shaped configuration having a base and an extended part having a predetermined diameter (107/106 in Fig. 1; Col. 4, line 54), and
- the contact area having a shortest linear dimension of about 2.0 mils (Col. 4, line 40) and the diameter of the pin being 0.25 mils (Col. 4, line 53) such that the diameter of the pin is no greater than half of the shortest linear dimension of the contact area.

Regarding claim 106, Khandros et al. substantially teach the entire claimed structure as applied to claims 105 and 52 above, including the part extending from the base having the pin configuration (106 in Fig. 1).

Regarding claim 107, Khandros et al. substantially teach the entire claimed structure as applied to claim 105 above, and further teach the extended part of the pin contact being adapted for a variety of flexible, resilient and detachably receivable/removable configurations for test and burn-in applications (Fig. 1-38; Col. 4-23).

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Response to Arguments

5. Applicant's arguments with respect to claims 52-60, 62-71 and 105-107 have been considered but are most in view of the new ground(s) of rejection.

6. Regarding claim 61, applicant contends that one of ordinary skill in the art would understand the conditions of "maximum thermal cycling".

However, as explained above, thermal cycling is performed under a wide range of parameters such as temperature, time, ramp rate, cycle/frequency, etc. It is not clear from the description in the specification what conditions and parameters are referred to define the conditions of the "maximum thermal cycling" so that a dimensional comparison and an evaluation of the difference in the length dimension with respect to the CNP of the substrate can be made.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310 (Right FAX) for After Final communications and 703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh NP

06-21-03

TOM THOMAS SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2800